Docket No.: S1022.81243US00
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Catherine Robert et al.
Serial No.:	10/535,063
Confirmation No.:	1852
Filed:	May 9, 2006
For:	TRANSMISSION OF A DIGITAL MESSAGE BETWEEN A MICROPROCESSOR MONITORING CIRCUIT AND AN ANALYSIS TOOL
Examiner:	J. R. Moll
Art Unit:	2181

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Dated: December 19, 2008
Jeanne Clark

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants request review of the rejections in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal.

REMARKS

The claims in this application stand rejected under 35 U.S.C. §103. These rejections are appropriate for consideration under the Pre-Appeal Brief Conference Program, as established at 1296 *Off. Gaz. Pat. Office* 67 (July 12, 2005), because they are based on clear errors in applying the law.

The Final Office Action mailed August 20, 2008 rejected claims 1-7 under 35 U.S.C. §103(a) as purportedly being obvious over U.S. Patent No. 6,961,875 ("Floyd") in view of U.S. Patent No. 6,070,210 ("Cheon").

Applicants respectfully submit that these rejections are based on clear errors in applying the law.

1. The Cited References Fail to Disclose All of the Claim Limitations

MPEP §2143 lists several examples of rationales that may be used to establish a *prima facie* case of obviousness. The Final Office Action appears to rely on the first rationale, "(A) combining prior art elements according to known methods to yield predictable results," in support of the assertion that independent claims 1 and 5 are purportedly rendered obvious by Floyd and Cheon.

Section A of MPEP §2143 describes in detail the requirement for rejecting a claim based on this rationale. This section of the MPEP states that the Office Action **must** articulate, *inter alia*, the following: (1) a finding that the prior art included each element claimed, although not necessarily in a single prior art reference, with the only difference between the claimed invention and the prior art being the lack of actual combination of the elements in a single prior art reference.

The Final Office Action has failed to establish a *prima facie* case of obviousness, because the first requirement set forth in MPEP §2143(A) is not met. Specifically, the Office Action fails to establish that the cited prior art taken as a whole includes each claimed element recited in each of independent claim 1 and 5.

For example, the cited references fail to disclose or suggest "processing first digital messages and the at least one second digital message via the analysis tool to analyze operation of the microprocessor, including determining the instruction sequence executed by the

microprocessor," as recited in each of claims 1 and 5 (see discussion on pages 8 and 9 of Applicants' response dated October 27, 2008).

The Final Office Action asserts that Floyd discloses first digital messages as the addresses 204 transferred from counter 202 to the trace array 207 via address decoder 203 (Final Office Action, page 2). However, these addresses are not first digital messages representative of first specific events which depend on execution of an instruction sequence by a microprocessor, as recited in each of claims 1 and 5. Rather, the addresses merely indicate the location in which the input logic signals are to be stored in the trace array, and ***do not reflect in any way whatsoever, an instruction sequence of a microprocessor.*** Accordingly, the trace array cannot use the addresses to infer anything about an instruction sequence of a microprocessor. In contrast, the first digital messages recited in claims 1 and 5 may be used by the analysis tool to analyze operation of the microprocessor, including determining the instruction sequence executed by the microprocessor.

The trace array of Floyd receives as input the addresses 204 and the input logic signals 205. The Advisory Action states, "clearly the trace array 207 determines the instruction sequence (by definition, a trace is a sequence of instructions)....Therefore, the first and second messages (control signals for the trace array) are sent in order to make the trace array function and therefore they are sent to determine the instruction sequence" (Advisory Action, page 2).

However, as discussed in Applicants' response dated October 27, 2008, the addresses 204 of Floyd only indicate the location in which the input logic signals 205 are to be stored in the trace array, and do not reflect in any way, an instruction sequence of a microprocessor. Furthermore, the Final Office Action and the Advisory Action appear to assert that the input logic signals 205 of Floyd form an instruction trace (Final Office Action, page 3; Advisory Action, page 2).

Applicants respectfully disagree that an **instruction sequence executed by a microprocessor** may be determined based upon the input logic signals of Floyd. Rather, the input logic signals in Floyd characterize the binary state of selected control and/or data signal values in the logic unit of a VLSI chip at a particular point in time (Floyd, col. 1, lines 49-55). The individual values of each of the input logical signals is considered when determining why an error signal in the VLSI chip was generated, but collectively, the sequence or trace of input logic

signals has no higher level cohesive meaning, such that analysis of a trace could be used to determine an **instruction sequence executed by the microprocessor**. In contrast, the first digital messages in embodiments of the present invention, and recited in claims 1 and 5, contain information that allows the analysis tool to determine an instruction sequence executed by the microprocessor.

Cheon fails to cure these deficiencies of Floyd. As discussed in Applicants' response dated May 6, 2008, Cheon fails to disclose or suggest determining an instruction sequence executed by a microprocessor. In Cheon, a microprocessor sends a "low" state or "high" state mode selection control signal to buffers 210 and 220 in circuitry associated with the DMA device to enable or disable acknowledgement signals DACK and BACK transferred between the SCSI controller and the DMA device. The state of the mode selection control signal, and thus which acknowledgement signal is active, determines the timing mode (i.e., single vs. burst mode) used to transfer data from the DMA device to the memory (Cheon, Fig. 2 and accompanying text at col. 3, line 65 – col. 4 line 26). Clearly this single control signal sent by the microprocessor of Cheon to change the timing mode of data transfer cannot be used by the memory to determine an instruction sequence executed by the microprocessor, as recited in claims 1 and 5.

As neither Floyd nor Cheon discloses or suggests the Office Action fails to satisfy the requirements for establishing a *prima facie* case of obviousness under 35 U.S.C. §103 regarding claims 1 and 5. Accordingly, the rejection of each of claims 1 and 5 is improper, and should be withdrawn.

2. The Result of Combining Various Reference Elements is Not Predictable

Even if all elements of each of Applicants' independent claims were found in the cited references, which they are not, the Final Office Action nonetheless has failed to meet the additional requirements set forth in MPEP §2143(A).

Specifically, MPEP §2143(A) further requires that to establish a *prima facie* case of obviousness the Office Action must articulate a finding that one of ordinary skill in the art could have combined the claimed elements by known methods, and with no change in their respective functions. The Office Action also must articulate a further finding that the results of the

combination would have been recognized as predicable to one of ordinary skill in the art. The Office Action has not met either of these requirements.

It is completely unclear from the Final Office Action how one of ordinary skill in the art would effectively combined the disparate teachings of the cited references to arrive at any result commensurate with the scope of Applicants' independent claims. The cited references are directed to respectively different problems, and solve their different problems by respectively different solutions. Floyd is directed to periodically recording control and data signals from a logic unit of a VLSI chip to a trace array. In contrast, Cheon is directed to a direct memory access (DMA) system. The Final Office Action has completely failed to articulate how one of ordinary skill would somehow implement a protocol to send an acknowledgement signal to the event sequence logic 232 of Floyd in response to making a determination that a memory is available for being written to as taught by Cheon, *without any change in functionality of Cheon's memory availability determination or acknowledgment signal and to achieve predictable results commensurate in scope with Applicants' independent claims.*

Absent any such discussion in the Final Office Action to this effect, again the Final Office Action has failed to meet its burden with respect to the requirements set forth in MPEP §2143(A). For these additional reasons, the rejection is improper and should be withdrawn.

Conclusion

The rejections of Applicants' claims 1-7 under 35 U.S.C. §103 clearly are erroneous, and Applicants respectfully request that the panel reverse these rejections.

Dated: December 19, 2008

Respectfully submitted,

By: _____

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